REMARKS

The Examiner's Action mailed on August 14, 2002 has been received and its contents carefully considered.

In this Amendment, Applicants have editorially amended the specification, revised the original drawings in accordance with the Examiner's comments, canceled claims 16-20 and amended claims 1, 5, 6, 8, 9, 10, 11, 12 and 15. Claims 1, 8 and 12 are the independent claims. Claims 1-15 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has noted informalities in the drawings, and has requested that corrected drawings be submitted. In response thereto, submitted concurrently with this Amendment are revised Formal Drawings, which include the changes required by the Examiner's Action. It is requested that this objection be withdrawn.

The Examiner has rejected various ones of the claims as being indefinite. In response thereto, the claims have been thoroughly amended to correct the matters specifically noted by the Examiner, and to correct various informalities noted during the review. It is submitted that the claims comply with all official provisions, and it is requested that this rejection be withdrawn.

The Examiner has rejected claims 1-4, 6-8, 10, and 12-15 as being anticipated by *Mori* (USP 5,903,049). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

Applicants' independent claim 1 is directed to a rearrangement sheet. The rearrangement sheet includes an insulating sheet that has an element mounting region defined thereon. The rearrangement sheet further includes conductive metallic patterns

formed on the insulating sheet, with the conductive metallic patterns surrounding, and not extending into, the element mounting region. This claimed configuration facilitates the connection between, for example, the bonding pads of a second element that is mountable on the rearrangement sheet, and bonding posts formed on a substrate. As such, no consideration of the effect of the positions of any metal wires that may connect bonding pads of a first element with the bonding posts of the substrate needs to be taken. This increases the degree of design freedom of the second element, as discussed in Applicants' specification on page 5, line 26, through page 6, line 9. Moreover, by ensuring that the conductive metallic patterns do not extend into the element mounting region, the overall configuration of the resulting semiconductor device can be made smaller, since the height of the conductive metallic pattern will not add to the overall height of the resulting device. This claimed rearrangement sheet is neither disclosed nor suggested by the cited reference.

Mori discloses a semiconductor module having semiconductor packages. In particular, this reference discloses providing two semiconductor elements 1a, 1b, which are connected to wiring patterns 3a, 3b, on a substrate 2a, 2b. The Examiner's Action has equated the wiring patterns 3a as being conductive metal patterns, such as recited in Applicants' independent claim 1. However, as is clear by the drawing in Figure 1, these so-called conductive metallic patterns 3a extend well into an element mounting region, i.e., the region that accommodates the element 1a, which is in contrast to the arrangement required by Applicants' claim 1. Moreover, this reference specifically teaches away from Applicants' configuration, since the so-called conductive metallic patterns 3a must extend underneath the element 1a and into the element mounting

region so as to be coupled to the bump 4a. As such, it is submitted that Applicants' independent claim 1, and the claims dependent therefrom, have not been anticipated by or otherwise rendered obvious by the cited reference.

Furthermore, Applicants' independent claim 8 is directed to a semiconductor device that includes *inter alia*, a rearrangement sheet that includes conductive metallic patterns that surround, and which do not extend under, a second element. This recitation is similar to that found within independent claim 1. As argued above with respect to independent claim 1, the cited reference does not disclose, and in fact teaches away from this configuration. As such, it is requested that this claim and the claims dependent therefrom be allowed.

Applicants' independent claim 12 is directed to a semiconductor device which includes a rearrangement sheet that is stuck onto an upper surface of a semiconductor element other than in a region where the bonding pads are formed, so as to be surrounded by the bonding pads. This claim also recites that the conductive metallic patterns of the rearrangement sheet include rearrangement posts, wire connection portions and rewiring leads. The Examiner's Action has not addressed these claimed features, except to state that the reference discloses rearrangement posts of the same number as the bonding pads. However, it is noted that to the extent that this reference may even disclose a rearrangement post, there is no disclosure or suggestion from this reference that such rearrangement posts are arranged so as to be surrounded by wire connection portions of the rearrangement sheet, as recited in claim 12.

Furthermore, claim 12 recites that conductive posts are formed on an upper surface of the rearrangement post. Part of the conductive posts is exposed from the

sealed portion. The Examiner's Action has not addressed these features, and it is further noted that the cited reference does not disclose or suggest such conductive posts, nor part of conductive posts being exposed from a sealed portion, as recited in claim 12. As such, it is submitted that Applicants' independent claim 12, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited reference. It is requested that these claims be allowed. It is further requested that these rejections be withdrawn.

The Examiner has further rejected claims 5, 9 and 11 as being obvious over *Mori* in view of *Verma et al.* (USP 6,407,450). Because *Verma et al.* do not overcome the deficiencies of *Mori*, it is submitted that claims 5, 9 and 11 are patentably distinguishable over the cited combination of references for at least the same reasons as independent claims 1 and 8, from which these claims respectively depend, as well as for the additional features recited therein. It is requested that these claims be allowed and that this rejection be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 4, line 19, through line 20, please replace the current paragraph with the following replacement paragraph:

--[Other] Another object of the present invention is to provide a method of manufacturing such a device easily and at low cost.--

Page 12, line 12, through line 16, please replace the current paragraph with the following replacement paragraph:

--Sealing portion 50 is formed so as to effect sealing by molded resin 48 so as to cover first element 14, rearrangement sheet 26 [for rearrangement], second element 16, first wires 46, first relay wires 42 and second relay wires 44 on the upper surface of substrate 12.--

IN THE CLAIMS:

Please cancel claims 16-20 without prejudice or disclaimer to the subject matter recited therein.

Please amend the claims as follows:

1. (Amended) A rearrangement sheet comprising an insulating sheet, said insulating sheet having an element mounting region defined thereon; and

conductive metallic patterns formed on [this] the insulating sheet so as to surround, and not extend into, the element mounting region.

5. (Amended) The rearrangement sheet according to claim 4, wherein said conductive metallic patterns comprise a laminated pattern of an underlying plated pattern formed on [the] an upper surface of the insulating sheet and a conductive metal plated pattern formed on this underlying plated pattern.

6. (Amended) The rearrangement sheet according to claim 1, wherein [an element mounting region is provided in a region on said insulating sheet other than the region where said conductive metallic patterns are formed, and] an insulating adhesive sheet is provided in [this] the element mounting region.

8. (Amended) A semiconductor device comprising:

a substrate;

a first element provided with a plurality of first bonding pads, and being disposed in a first element formation region [formed] on [the] an upper surface of [this] the substrate;

a second element provided with a plurality of second bonding pads, the second element being disposed over an [formed on the] upper side of [this] the first element;

a plurality of bonding posts provided [in a region of] on the upper surface of said substrate [other than] , and outside so as to surround the first element formation region;

first wires that connect [post for first pad connection,] respective ones of the bonding posts[, and first pads for bonding post connection,] with respective ones of said first bonding pads; and

[wherein] a rearrangement sheet provided with an insulating sheet, and a plurality of conductive metallic patterns that are formed on [this] the insulating sheet, [is] the rearrangement sheet being provided between said first element and said second element;

wherein said conductive metallic patterns are formed in a region[, which is a region on said insulating sheet] exposed from said second element, so that the conductive metallic patterns surround, and do not extend under, the second element, [comprising] said conductive metallic patterns each including a first portion [position] that can be reached by [the] a straight line extending from another respective one of the bonding posts [a post] for a second pad connection, [of said bonding posts,] without contacting or crossing said first bonding pads, and a second [position] portion, capable of wire bonding with a respective one of the second bonding pads, [for] thereby coupling the another respective one of the bonding post [connection, of said] to the second bonding pad [pads];

[these conductive metallic patterns] the first portions and [said post for second pad connection are] the respective another ones of the bonding posts being connected by first relay wires; and

said [conductive metallic patterns] second portion and said [second pads for bonding post connection are] respective ones of the second bonding pads being connected by second relay wires.

9. (Amended) The semiconductor device according to claim 8, wherein said conductive metallic patterns [are constituted by] include an underlying plated pattern formed on [the] an upper surface of said insulating sheet, and a conductive metal plated pattern formed on [this] the underlying plated pattern.

10. (Amended) The semiconductor device according to claim 8, wherein said conductive metallic patterns are metallic wiring patterns formed on [the] an upper surface of said insulating sheet.

11. (Amended) The semiconductor device according to claim 8, wherein said conductive metallic patterns comprise a metallic wiring pattern formed on [the] an upper surface of said insulating sheet and conductive metal plated patterns provided on [these] the metallic wiring patterns [in a region] including [said] the first [position] portion and [in a region] including [said] the second [position] portion [separately or continuously].

12. (Amended) A semiconductor device, comprising:

a semiconductor element having a plurality of bonding pads formed on [the] an upper surface thereof;

a rearrangement sheet comprising an insulating sheet and conductive metallic patterns electrically connected with said bonding pads, stuck onto [a region of this] the upper surface of the semiconductor element other than in a [the] region where the bonding pads are formed so as to be surrounded by the bonding pads; and

a sealed portion that seals the upper surface of said semiconductor element so as to cover said rearrangement sheet;

wherein said conductive metallic patterns comprise rearrangement posts of [the] a same number as said bonding pads, wire connection portions of the same number as the bonding pads, the rearrangement posts and the wire connection portions being arranged so that the rearrangement posts are surrounded by the wire connection portions, and rewiring leads that connect said rearrangement posts and said wire connection portions;

said wire connection portions and said bonding pads are connected by metallic wires,

conductive posts are formed on [the] an upper surface of said rearrangement posts; and

part of [these] the conductive posts is exposed from said sealed portion.

15. (Amended) The semiconductor device according to claim 12, wherein, of said conductive metallic patterns, said rearrangement posts and said rewiring leads are constituted by [conductive] first metallic wiring patterns; and

said wire connection portions are constituted by [conductive] second metallic wiring patterns and conductive metal plated patterns formed on [these conductive] the second metallic wiring patterns.